AMENDMENTS TO THE CLAIMS

1. (Currently amended): A circuit for preventing transmission of a fixed pattern of an optical digital transmission equipment, comprising:

a memory for temporarily accumulating a low-order group signal,

a multiplexing circuit for multiplexing an output signal output by said memory with an overhead bit necessary for optical digital transmission, ~~and~~

a pattern generation circuit for generating an unfixed pattern having no fixed value and outputting the pattern to said multiplexing circuit~~.~~, and

a selection circuit coupled to said multiplexing circuit, said pattern generation circuit, and said memory, wherein in response to reception of said fixed pattern output by said memory, said selection circuit selects said unfixed pattern generated by said pattern generation circuit.

2. (Original): The circuit for preventing transmission of a fixed pattern of an optical digital transmission equipment according to claim 1, wherein

said unfixed pattern is applied to said multiplexing circuit while said memory outputs a fixed pattern.

3. (Canceled)

4. (Currently amended): The circuit for preventing transmission of a fixed pattern of an optical digital transmission equipment according to claim ~~3~~ 1, the circuit further comprising

a phase comparator coupled to said selection circuit, said phase comparator outputting a reset signal that resets said memory based on a phase difference between a phase of write to said memory and a phase of read from the memory, wherein in response

to said phase comparator, said selection circuit selects said unfixed pattern based on said reset signal output by said phase comparator.

5. (Currently amended): The circuit for preventing transmission of a fixed pattern of an optical digital transmission equipment according to claim ~~3~~ 1, further comprising

a phase comparator for comparing a phase difference between a phase of write to said memory and a phase of read from the memory and when said phase difference is larger than a set value set in advance, outputting a reset signal which resets said memory, wherein

said selection circuit selects said unfixed pattern based on said reset signal.

6. (Original): The circuit for preventing transmission of a fixed pattern of an optical digital transmission equipment according to claim 4, further comprising

a reset signal detection circuit for outputting a switching signal based on a read address signal applied to said memory from when said memory is reset until when a signal first written into said memory is read from said memory, wherein

said selection circuit selects said unfixed pattern based on said reset signal and said switching signal.

7. (Original): The circuit for preventing transmission of a fixed pattern of an optical digital transmission equipment according to claim 4, further comprising

a reset signal detection circuit for detecting said reset signal, wherein

a read address signal applied to said memory is also applied to said reset signal detection circuit,

said reset signal detection circuit outputs a switching signal based on said read address signal from when said memory is reset until when a signal first written into said memory is read from said memory, and

said selection circuit selects said unfixed pattern based on said reset signal and said switching signal.

8. (Original): The circuit for preventing transmission of a fixed pattern of an optical digital transmission equipment according to claim 6, further comprising

a determination circuit and an OR circuit, wherein

said determination circuit is provided between said OR circuit and an input side of said memory,

said determination circuit outputs a switch signal when a signal written into said memory has a fixed pattern for a set time,

to said OR circuit, said switching signal and said switch signal are applied, and

said selection circuit selects said unfixed pattern based on said switch signal in addition to said reset signal and said switching signal.

9. (Original): The circuit for preventing transmission of a fixed pattern of an optical digital transmission equipment according to claim 1, wherein

said unfixed pattern is a random pattern.

10. (Original): A circuit for preventing transmission of a fixed pattern of an optical digital transmission equipment, comprising:

a memory for temporarily storing data,

a multiplexing circuit for multiplexing a signal output by said memory with an overhead bit necessary for optical digital transmission,

a pattern generation circuit for generating an unfixed pattern having no fixed value and outputting the pattern to said multiplexing circuit,

a selection circuit coupled to said multiplexing circuit, said pattern generation circuit, and said memory, wherein in response to reception of said fixed pattern output by

said memory, said selection circuit selects said unfixed pattern generated by said pattern generation circuit,

an E/O conversion unit for converting a signal output by said multiplexing circuit into an optical signal,

an optical fiber for transmitting an optical signal output by said E/O conversion unit, and

an O/E conversion unit for converting an optical signal output by said optical fiber into an electric signal, wherein

while said memory outputs a fixed pattern, the unfixed pattern is applied to said multiplexing circuit.

11. (Original): The circuit for preventing transmission of a fixed pattern of an optical digital transmission equipment according to claim 10, wherein

said unfixed pattern is a random pattern.

12. (Canceled)

13. (Currently amended): The circuit for preventing transmission of a fixed pattern of an optical digital transmission equipment according to claim ~~12~~ 10, further comprising

a phase comparator for outputting a reset signal which resets said memory based on a phase difference between a phase of write to said memory and a phase of read from the memory, wherein

said selection circuit selects said unfixed pattern based on said reset signal.

14. (Currently amended): The circuit for preventing transmission of a fixed pattern of an optical digital transmission equipment according to claim ~~12~~ 10, the circuit further comprising

a phase comparator coupled to said selection circuit, said phase comparator comparing a phase difference between a phase of write to said memory and a phase of read from the memory and when said phase difference is larger than a set value set in advance, outputting a reset signal that resets said memory,

wherein, in response to said phase comparator, said selection circuit selects said unfixed pattern based on said reset signal output by said phase comparator.

15. (Original): The circuit for preventing transmission of a fixed pattern of an optical digital transmission equipment according to claim 13, further comprising

a reset signal detection circuit for outputting a switching signal based on a read address signal applied to said memory from when said memory is reset until when a signal first written into said memory is read from said memory, wherein

said selection circuit selects said unfixed pattern based on said reset signal and said switching signal.

16. (Original): The circuit for preventing transmission of a fixed pattern of an optical digital transmission equipment according to claim 13, further comprising

a reset signal detection circuit for detecting said reset signal, wherein

a read address signal applied to said memory is also applied to said reset signal detection circuit,

said reset signal detection circuit outputs a switching signal based on said read address signal from when said memory is reset until when a signal first written into said memory is read from said memory, and

said selection circuit selects said unfixed pattern based on said reset signal and said switching signal.

17. (Original): The circuit for preventing transmission of a fixed pattern of an optical digital transmission equipment according to claim 15, further comprising

a determination circuit and an OR circuit, wherein

said determination circuit is provided between said OR circuit and an input side of said memory,

said determination circuit outputs a switch signal when a signal written into said memory has a fixed pattern for a set time,

to said OR circuit, said switching signal and said switch signal are applied, and

said selection circuit selects said unfixed pattern based on said switch signal in addition to said reset signal and said switching signal.